ABSTRACT OF THE DISCLOSURE

A conditional clock buffer circuit includes a clock output and is coupled to receive a clock input and a condition signal. The conditional clock buffer circuit includes a first circuit coupled to receive the clock input and a second circuit coupled to receive the clock input and the condition signal. The first circuit is configured to generate a first state on the clock output responsive to a first phase of the clock input. The second circuit is configured to conditionally generate a second state on the clock output responsive to the condition signal during a first portion of a second phase of the clock input. In one implementation, one or more of the conditional clock buffer circuits may be included in a clock tree. The clock tree may also include one or more levels of buffering.